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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/877,027	06/11/2001	Yasuhiko Tsukikawa	57454-138	9823

7590 03/24/2003

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EXAMINER	
NGUYEN, LINH M	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/877,027	TSUKIKAWA, YASUHIKO	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/21/2003 and 03/10/2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-13* is/are allowed.

6)☒ Claim(s) *1 and 4-14* is/are rejected.

7)☒ Claim(s) *2,3,5-10 and 15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *10 & 12* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This is a reply to the Applicant's amendments submitted on 01/21/2003 and 03/10/2003. According to this amendment, claims 1-17 are now presented in this instant application.

Upon reviewing the Response corresponding to the Office Action mailed, an inadvertent processing error has been found; in particular, the content therein belongs to a un-updated version. An apology is hereby extended for any confusion having been caused.

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 11/13/2002 is in compliance with the provisions of 37 CFR 1.97 and 1.98. Accordingly, the information disclosure statement is being considered by the examiner.

2. The information disclosure statement (IDS) submitted on 01/06/2003 is not considered due to: (i) reference 6,247,138 (Tamura et al.) is already included in the information disclosure statement (IDS) submitted on 11/13/2002, and (ii) lack of a copy of foreign patent No. 387,065.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Goldenberg et al. (WO 94/15401 of record).

With respect to claim 1, Goldenberg et al. discloses, in figure 1, a delay locked loop circuit comprising (1) a delay circuit [44.(N-1), 44. (N-2), 44.2, 44.1, 40, 50] for delaying a first clock signal [42] and outputting a second clock signal [output of 50], (2) a detector [56] for detecting which of the first and second clocks is advanced in a phase, and (3) a gray code counter [36] using a gray code and being responsive (via RESET) to an output of the detector [56] for selectively generating one of a signal [38] to increase (via RESET) an amount of delay of the delay circuit and a signal to decrease the amount of delay of the delay circuit; in which the output of the detector indicates that the first clock is in advance of the second clock in a phase or the second clock is in advance of the first clock in a phase.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goldenberg et al. (WO 94/15401 of record), in view of Taniguchi et al. (U.S. Patent No. 6,225,843 of record).

With respect to claim 4 and 14, Goldenberg et al. discloses, in figure 1, a digitally controlled phase shifter system and a corresponding control method for the system; the digitally controlled phase shifter comprises a delay locked loop circuit including (1) an external clock [42], (2) a delay circuit [44.(N-1), 44. (N-2), 44.2, 44.1, 40, 50] for delaying the first clock signal [42] and outputting a second clock signal [output of 50], (3) a detector [56] for detecting which

of the first and second clocks is advanced in a phase, and (4) a gray code counter [36] using a gray code and being responsive (via RESET) to an output of the detector [56] for selectively generating a signal [38] to increase (via RESET) an amount of delay of the delay circuit and a signal to decrease the amount of delay of the delay circuit; in which the output of the detector indicates that the first clock is in advance of the second clock in a phase or the second clock is in advance of the first clock in a phase.

Goldenberg et al.'s teachings lack an input buffer for receiving the external clock and outputting the first internal clock.

Taniguchi et al. discloses, in Fig. 3, a delay locked loop circuit using an input buffer [22] for receiving an external clock [CLK] and generating a first internal clock [N3] (see col. 4, lines 25-28).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the delay locked loop circuit of Goldenberg et al. by additionally configuring an input buffer as taught by Taniguchi et al. for reshaping the external clock signal since such an arrangement of the input buffer for receiving the external clock signal would provide a strong signal, e.g. signal without noise interference, etc., to be inputted to the delay circuits, and thus improve signal synchronization at the output.

Allowable Subject Matter

6. Claims 11-13 are allowed.

7. Claims 2-3, 5-10, and 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Prior art of record does not show or fairly suggest:

(i) a gray code counter including (a) a gray code register for storing the gray code, (b) a binary code converter for converting the gray code into a binary code, (c) an upward carry/downward carry generator using the binary code stored in the binary code converter, to generate an upward carry signal and a downward carry signal, and (d) a carry multiplexer for generating from the upward carry signal and the downward carry signal a carry signal corresponding to a result obtained by the detector, for updating said gray code in the gray code register, as called for in claims 2, 5, and the corresponding steps, as called for in claim 15; and

(ii) a delay locked loop including a combination of (a) a first input buffer for receiving at least a first external clock and a second external clock complementary in phase to the first external clock, and outputting a first internal clock at the timing of the rising edge of the first external clock when a potential of the first external clock is equal to that of the second external clock, (b) a second input buffer for receiving at least the first and second external clocks, and outputting a second internal clock at the timing of the rising edge of the second external clock when a potential of the first external clock is equal to that of the second external clock, and (c) a second delay circuit for delaying the second internal clock to output a fourth internal clock, as called for in claim 11.

Remarks and conclusion

8. Applicant's arguments with respect to claims 1, 4, and 14 have been considered but are moot in view of the new ground(s) of rejection.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (703) 305-0414. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703) 308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-0142 for regular communications and (703) 305-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Linh M. Nguyen
Examiner
Art Unit 2816

LMN
March 21, 2003